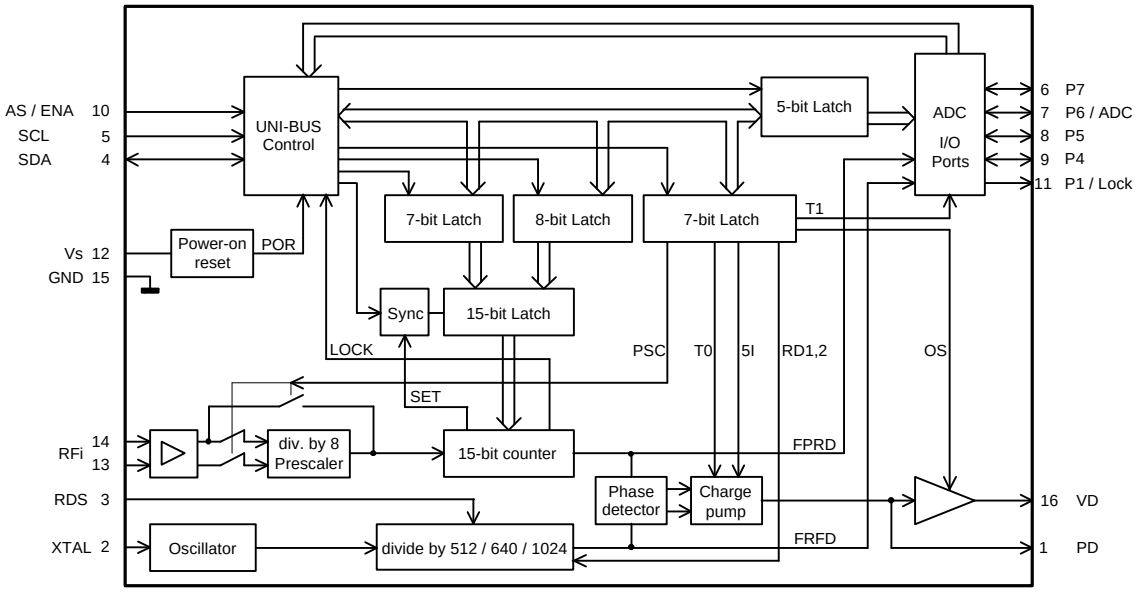
Frequency Synthesizer for TV Tuner with UNIVERSAL BUS

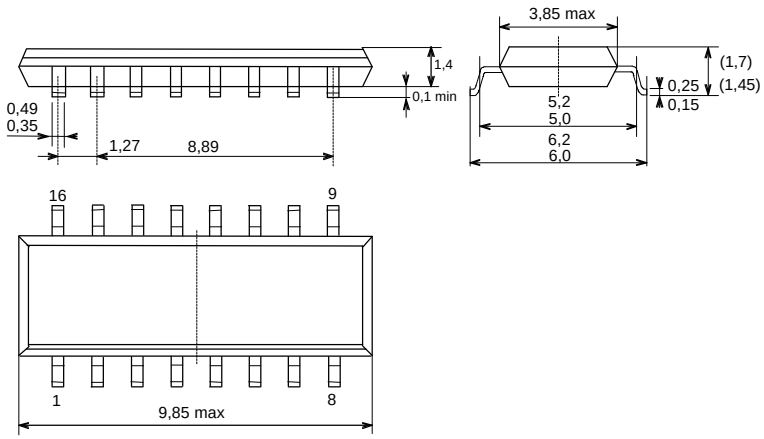
FEATURES

- 1.3 GHz divide-by-8 prescaler integrated (can be bridged)
- UNIVERSAL BUS: I²C - Bus **or** 3 - wire - Bus
  I²C - Bus software compatible to U 6204 B
  3 - wire - Bus software compatible to U 6358 B
- I²C - Bus Mode: 4 bidirectional ports (open collector)
  1 unidirectional port (open collector)
  5 level ADC
  4 addresses selectable at pin10
- 3 - Wire Bus Mode: 4 unidirectional ports (open collector)
  Lock output (open collector)
- Low power consumption (typ. 5 V / 35 mA)
- Electrostatic protection according to MIL - STD 883
- SO - 16 small package

BLOCK DIAGRAM

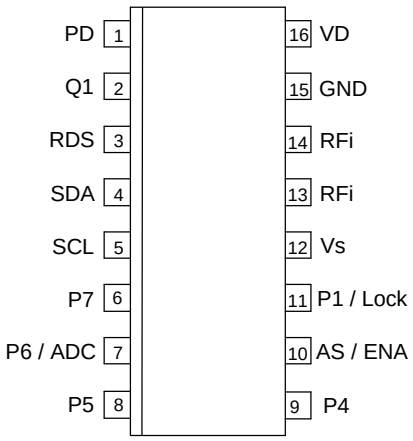


PACKAGE SO - 16 small (All dimensions in mm)



PIN CONFIGURATION

PIN	SYMBOL	FUNCTION
1	PD	Charge pump output
2	Q1	XTAL
3	RDS	Reference divider select input
4	SDA	Data input / output
5	SCL	Clock input
6	P7	Input / output port
7	P6 / ADC	Output port / ADC input
8	P5	Input / output port
9	P4	Input / output port
10	AS / ENA	Address select / Enable input
11	P1 / Lock	Port output / Lock output
12	Vs	Supply voltage
13	RFi	RF input
14	RFi	RF input
15	GND	Ground
16	VD	Active filter output



DESCRIPTION

The U6214B is a single chip PLL designed for TV and VCR receiver systems. It consists of an bridgeable divide-by-8 prescaler with an integrated preamplifier, a 15bit programmable divider, a crystal oscillator and a reference divider with three selectable divider ratios (÷512 / ÷640 / ÷1024), a phase / frequency detector together with a charge-pump, which is driving the tuning amplifier. Only one external transistor is required for varactor line driving. The device can be controlled via I²C-bus format or 3-wire-bus format. It detects ***automatically*** which bus format is received, therefore there is no need for a bus selection pin. In I²C-bus mode the device has four programmable addresses, programmed by applying a specific input voltage to the address select input, enabling the use of up to four synthesizers in a system. The same pin serves in 3-wire-bus mode as the enable signal input. There are five open collector outputs for switching functions available. In 3-wire-bus mode there are four open collector outputs and one serves as Locksignal output. All open collector outputs are capable of sinking at least 10 mA. In I²C-bus mode there is an Analog-to-Digital Converter available for digital AFC control applications and the ports P4, P5 and P7 can be used as inputs.

FUNCTIONAL DESCRIPTION

The U6214B is programmed via 2-wire I²C bus or 3-wire bus depending on the received data format. The three bus inputs pin 4,5,10 are used as *SDA, SCL* and *address select* inputs in I²C-bus mode or as *data, clock* and *enable* inputs in 3-wire bus mode. The data includes the scaling factor SF and switching output information. In I²C-bus mode there are some additional functions available (ADC, bidirectional ports, etc.).

Oscillator frequency calculation : fvco = PSF * SPF * frefosc / SRF

fvco: Locked frequency of voltage controlled oscillator

PSF : Scaling factor of prescaler (÷1 or ÷8 in I²C- / ÷8 in 3-wire bus mode)

SPF : Scaling factor of programmable divider (15bit)

SRF : Scaling factor of reference divider (÷512 / ÷640 / ÷1024)

frefosc : Reference oscillator frequency: 3.2 / 4 MHz crystal or external reference frequency

The input amplifier together with a divide-by-8 prescaler gives an excellent sensitivity (see 'TYPICAL PRESCALER INPUT SENSITIVITY'). The input impedance is shown in the diagram 'TYPICAL INPUT IMPEDANCE'. When a new divider ratio according to the requested fvco is entered, the phase detector and charge pump together with the tuning amplifier adjusts the control voltage of the VCO until the output signals of the programmable divider and the reference divider are in frequency and phase locked. The reference frequency may be provided by an external source capacitively coupled into pin 2, or by using an on-board crystal with an 18pF capacitor in series. The crystal operates in the series resonance mode. The reference divider division ratio is selectable to ÷512 / ÷640 / ÷1024. Therefore with a 4MHz crystal and the nominal division ratio of 512 of the

reference divider the comparison frequency is 7.8125kHz, which gives 62.5kHz steps for the VCO, or with a 3.2MHz crystal respectively 6.25kHz comparison frequency and 50kHz VCO step size. In I²C-bus-mode the divison ratio may be set via two bits, in 3-wire-bus-mode via a voltage at pin 3. In addition there are port outputs available for bandswitching and other purposes.

APPLICATION

A typical application is shown on page 15. All input / output interface circuits are shown on page 14. Some special features which are related to test- and alignment procedures for tuner production are explained in the following bus mode description.

ABSOLUTE MAXIMUM RATINGS

All voltages are referred to GND (pin 15).

PARAMETER	SYMBOL	PIN	CONDITIONS	MIN.	MAX.	UNIT
Supply voltage	Vs	12		-0.3	6	V
RF input voltage	RFi	13,14		-0.3	Vs+0.3	V
Xtal input voltage	Q1	2		-0.3	Vs+0.3	V
Charge pump output voltage	PD	1		-0.3	Vs+0.3	V
Active filter output voltage	VD	16		-0.3	Vs+0.3	V
Bus input/output voltage	VSDA, VSCL	4,5		-0.3	6	V
SDA output current	ISDA	4	open collector	-1	5	mA
Address select / ENA input	VAS / ENA	10		-0.3	Vs+0.3	V
Port output current	P1, P4-7	6-11	open collector	-1	15	mA
Total port output current	P1, P4-7	6-11	open collector	-1	50	mA
Port input / output voltage	P1, P4-7	6-11	in off state	-0.3	15	V
Port output voltage	P1, P4-7	6-11	in on state	-0.3	6	V
Junction temperature	Tjmax			-40	125	°C
Storage temperature	Tstor			-40	125	°C

OPERATING RANGE

All voltages are referred to GND (pin 15).

PARAMETER	SYMBOL	PIN	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supply voltage	Vs	12		4.5	5	5.5	V
Ambient temperature	Tamb			0		70	°C
Input frequency	RFi	13,14	PSC = 1	80		1300	MHz
Input frequency	RFi	13,14	PSC = 0	1		220	MHz
Programmable divider	SF			256		32767	
Xtal oscillator	fXtal	2		3	4	4.48	MHz
Thermal resistance	Rthja		SO - 16 small			110	K/W

ELECTRICAL CHARACTERISTICS

Test conditions (unless otherwise specified): Vs=5V, Tamb=25°C.

PARAMETER	SYMBOL	PIN	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supply current (prescaler on)	Is	12	P1, P4-7 = 0; PSC=1		35		mA
Supply current (prescaler off)	Is	12	P1, P4-7 = 0; PSC=0		21		mA
Input sensitivity							
f_{RFi} = 80 - 1000 MHz	Vi 1)	13	PSC = 1	10		315	mVrms
f_{RFi} = 1300 MHz	Vi 1)	13	PSC = 1	40		315	mVrms
f_{RFi} = 10 - 220 MHz	Vi 1)	13	PSC = 0	10		315	mVrms
Crystal oscillator							
Recommended crystal series resistance				10		200	Ω
Crystal oscillator drive level		2			50		mVrms
Crystal oscillator source impedance		2	Nominal spread ±15%		-650		Ω
External reference input frequency		2	AC coupled sinewave	3		4.5	MHz
External reference input amplitude		2	AC coupled sinewave	70		200	mVrms
Port outputs / lock output (open collector)	P4-7 P1, Lock	6-9 11	Lock condition : low				
Leakage current	IL		VH = 13.5 V			10	uA
Saturation voltage	VSL 2)		IL = 10 mA			0.5	V

Port inputs	P4,5,7	6,8,9					
Input voltage high	Vi 'H'			2.7			V
Input voltage low	Vi 'L'					0.8	V
Input current high	Ii 'H'		Vi 'H' = 13.5 V			10	µA
Input current low	Ii 'L'		Vi 'L' = 0 V	-10			µA

Notes : 1) RMS - voltage calculated from the measured available power on 50 Ω.

2) Tested with one port active. The collector voltage of an active port may not exceed 6V.

ELECTRICAL CHARACTERISTICS (continued)

Test conditions (unless otherwise specified): Vs=5V, Tamb=25°C.

PARAMETER	SYMBOL	PIN	CONDITIONS	MIN.	TYP.	MAX.	UNIT
ADC input	ADC	6	See page9 for ADC-levels				
Input current high	Ii 'H'		Vi 'H' = 13.5 V			10	µA
Input current low	Ii 'L'		Vi 'L' = 0 V	-10			µA
Charge pump output	PD						
Charge pump current 'H'	IPDH	1	5I = 1, VPD = 1.7 V		±180		µA
Charge pump current 'L'	IPDL	1	5I = 0, VPD = 1.7 V		±50		µA
Charge pump leakage current	IPDTRI	1	T0 = 1, VPD = 1.7 V		±5		nA
Charge pump amplifier gain		1,16			6400		
Bus inputs	SDA, SCL						
Input voltage high	Vi 'H'	4,5		3		5.5	V
Input voltage low	Vi 'L'	4,5				1.5	V
Input current high	Ii 'H'	4,5	Vi 'H' = Vs			10	uA
Input current low	Ii 'L'	4,5	Vi 'L' = 0 V	-20			uA
Output voltage SDA (open collector)	VSDA 'L'	4	ISDA'L' = 3 mA			0.4	V
Address selection / Enable input	AS / ENA	10					
Input current high	Ii 'H'		Vi 'H' = Vs			20	µA
Input current low	Ii 'L'		Vi 'L' = 0 V	-100			µA

I²C - BUS DESCRIPTION

FUNCTIONAL DESCRIPTION

When the U6214B is controlled via 2-wire I²C-bus format, then data and clock signals are fed into the SDA and SCL lines respectively. Depending on the LSB of the address byte the device can either accept new data (write mode: LSB = 0) or send data (read mode: LSB = 1). The device has four programmable I²C-bus addresses. The tables 'I²C-BUS WRITE DATA FORMAT' and 'I²C-BUS READ DATA FORMAT' describe the format of the data and show how to select the device address by applying a voltage at pin 10.

WRITE mode (Address byte LSB = 0)

When write mode is activated and the correct address byte is received, the SDA line is pulled low by the device during the acknowledge period, and then also during the acknowledge periods, when additional data bytes are programmed. After the address transmission (first byte), data bytes can be sent to the device. There are four data bytes requested to fully program the device. Once the correct address is received and acknowledged, the first bit of the following byte determines whether that byte is interpreted as byte 2 or 4; a logic 0 for divider information and a logic 1 for control and port output information. When byte 2 was received the device always expects byte 3 next. Likewise when byte 4 was received, byte 5 is expected. Additional data bytes can be entered without the need to re-address the device until an I²C-bus stop condition is recognised. This allows a smoth frequency sweep for fine tuning AFC purposes. The table 'I²C-BUS PULSE DIAGRAM' shows some possible data transfer examples.

The programmable divider bytes PDB1 and PDB2 are controlling the division ratio of the 15 bit programmable divider. They are loaded in a 15 bit latch after the 8th clock pulse of the second divider byte PDB2, the control and the port register latches are loaded after the 8th clock pulse of the control byte CB1 resp. port byte CB2.

The control Byte CB1 allows to control the following special functions:

- 5I - bit switches between low and high charge pump current
- T1 - bit enables divider test mode when it is set to logic 1
- T0 - bit allows to disable the charge pump when it is set to logic 1
- PSC - bit switches prescaler off when it is set to logic 0
- RD1 and RD2 - bit allow to select the reference divider ratio
- OS - bit disables the charge pump drive amplifier output when it is set to logic 1.

Only in I²C bus mode the charge pump current can be controlled. In 3-wire-bus mode there is always the high charge pump current active.

The OS-bit function disables the complete PLL function. This allows the tuner alignment by supplying the tuning voltage directly through the 30V supply voltage of the tuner.

The control byte CB2 programs the port outputs P1 and P4-7; a logic 0 for high impedance output (off) or a logic 1 for low impedance output (on). At power-on all ports are set to the high impedance state.

I²C - BUS DESCRIPTION (continued)

DESCRIPTION	I²C BUS *WRITE* DATA FORMAT								
	MSB								LSB
Address byte	1	1	0	0	0	AS1	AS2	**0**	A
Progr. divider byte 1	0	n14	n13	n12	n11	n10	n9	n8	A
Progr. divider byte 2	n7	n6	n5	n4	n3	n2	n1	n0	A
Control byte 1	1	5I	T1	T0	PSC	RD2	RD1	OS	A
Control byte 2	P7	P6	P5	P4	X	X	P1	X	A

A = Acknowledge ; X = not used ; Unused bits of controlbyte 2 should be 0 for lowest power consumption

n0..n14 :	Scaling factor (SF)	SF = 16384*n14 + 8192*n13 + ... + 2*n1 + n0	
PSC :	Prescaler on / off	PSC = 1 : prescaler on	PSC = 0 : prescaler off
T0, T1 :	Testmode selection	T1 = 1 : divider test mode on fPRD at pin6, fRFD at pin7	T1 = 0 : divider test mode off
		T0 = 1 : charge pump disable	T0 = 0 : charge pump enable
P1, P4-7 :	Port outputs	P1, P4-7 = 1 : open collector active	
5I :	Charge pump current switch	5I = 1 : high current	5I = 0 : low current
OS :	Output switch	OS = 1 : varicap drive disable	OS = 0 : varicap drive enable

RD1,RD2 : Reference divider selection

RD2	RD1	Reference divider ratio
X	0	640
0	1	1024
1	1	512

AS1,AS2 : Address selection pin 10

AS1	AS2	Address	Dec.value	Voltage at pin10
0	1	1	194	open
0	0	2	192	0 to 10% Vs
1	0	3	196	40 to 60% Vs
1	1	4	198	90% Vs to 13.5V

I²C - BUS DESCRIPTION (continued)

READ mode (Address byte LSB = 1)

After the address transmission (first byte), the status byte can be read from the device on the SDA line (MSB first). Data is valid on the SDA line during logic high of the SCL signal. The controller accepting the data has to pull the SDA line to low-level during all status byte acknowledge periods to read another status byte. If the controller fails to pull the SDA line to low-level during this period, the device will then release the SDA line to allow the controller to generate a STOP condition.

The POR-bit (power-on-reset) is set to a logic 1 when the supply voltage Vs of the device has dropped below 3V (at 25°C) and also when the device is initially turned on. The POR-bit is reset to a logic 0 when the read sequence is terminated by a STOP condition. When POR-bit is set high (at low Vs) it is indicated that all the programmed information is lost and the port outputs are all set to high impedance state.

The FL-bit indicates whether the loop is in phase lock condition (logic 1) or not (logic 0).

If the ADC or the ports are to be used as inputs the corresponding outputs must be programmed to a high impedance state (logic 0).

The bits I2, I1 and I0 show the status of the I/O ports P7, P5 and P4 respectively. A logic 0 indicates a LOW level and a logic 1 a HIGH level (TTL levels).

The bits A2, A1 and A0 represent the digital information of the 5 level ADC. This converter can be used to feed AFC information to the controller from the IF section of the receiver, as shown in the typical application circuit on page 15.

DESCRIPTION	I²C BUS *READ* DATA FORMAT								
	MSB								LSB
Address byte	1	1	0	0	0	AS1	AS2	**1**	A
Status byte	POR	FL	I2	I1	I0	A2	A1	A0	-

POR : Power-on-reset flag : POR = 1 on power on

FL : in-lock flag : FL = 1, when loop is phase locked

I2, I1, I0 : digital information of I/O-ports P7, P5 and P4 respectively

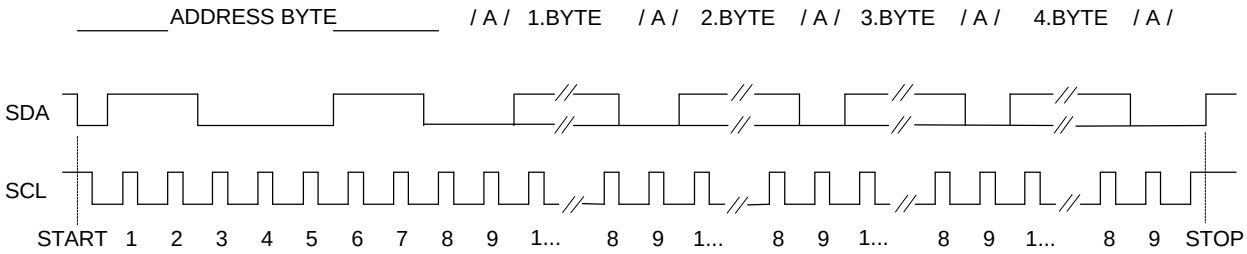
A2, A1, A0 : digital data of the 5-level ADC. see next table

A/D CONVERTER LEVELS :

A2	A1	A0	Input voltage to ADC pin 7
1	0	0	60% Vs to 13.5V
0	1	1	45% to 60% Vs
0	1	0	30% to 45% Vs
0	0	1	15% to 30% Vs
0	0	0	0V to 15% Vs

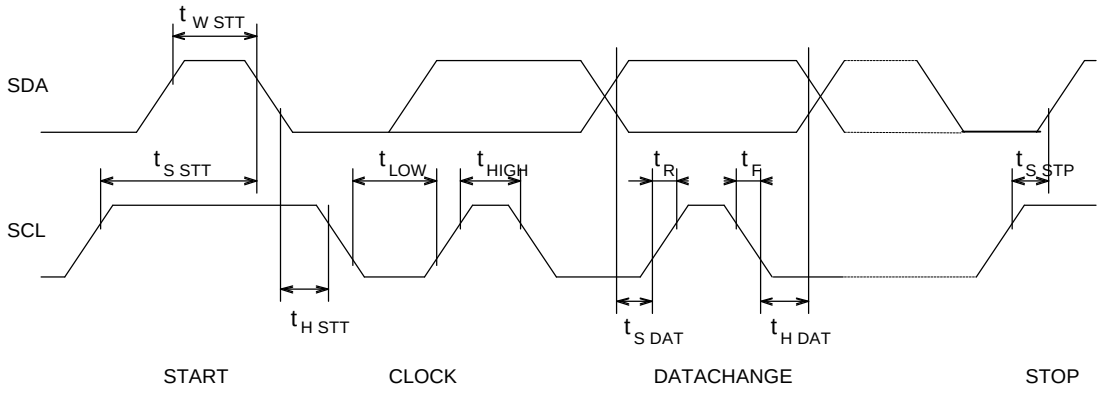
I²C - BUS DESCRIPTION (continued)

I²C - BUS PULSE DIAGRAM



Data transfer examples	Description
START - ADR - PDB1 - PDB2 - CB1 - CB2 - STOP	START = Start condition
START - ADR - CB1 - CB2 - PDB1 - PDB2 - STOP	ADR = Address byte
START - ADR - PDB1 - PDB2 - CB1 - STOP	PDB1 = Progr. divider byte 1
START - ADR - PDB1 - PDB2 - STOP	PDB2
START - ADR - CB1 - CB2 - STOP	CB1 = Progr. divider byte 2
START - ADR - CB1 - STOP	CB2
	STOP = Control byte 1
	= Control byte 2
	= Stop condition

I²C-BUS TIMING



PARAMETER	SYMBOL	CONDITIONS	MIN.	MAX.	UNIT
Rise time SDA, SCL	tR			15	µs
Fall time SDA, SCL	tF			15	µs
Clock frequency SCL	fSCL		0	100	kHz
Clock 'H' pulse	tHIGH		4		µs
Clock 'L' pulse	tLOW		4		µs

Hold time start	tH STT		4		µs
Waiting time start	tW STT		4		µs
Setup time start	tS STT		4		µs
Setup time stop	tS STP		4		µs
Setup time data	tS DAT		0.3		µs
Hold time data	tH DAT		0		µs

3 - WIRE - BUS DESCRIPTION

When the U6214B is controlled via 3-wire bus format, then data, clock and enable signals are fed into the SDA, SCL and AS/ENA lines respectively. The diagram '3 - WIRE - BUS PULSE DIAGRAM' shows the data format. The data consist of a single word, which contains the programmable divider (15bit) and port information. Only during the enable high period the data is clocked into the internal data shift register on the negative clock transition. During enable low periods the clock input is disabled. New data words are only accepted by the internal data latches from the shift register on a negative transition of the enable signal when exactly ninetheen clock pulses were sent during the high period of the enable. The data sequence and the timing is described in the following diagrams.

In 3-wire-bus mode pin 11 becomes automatically the Locksignal output. An improved lock detect circuit generates a flag when the loop has attained lock. 'In lock' is indicated by a low impedance state (on) of the open collector output.

In 3-wire-bus mode the following conditions are set internally:

- 5I = 1 : always high charge pump current active
- T1 = 0 : divider test mode off
- T0 = 0 : charge pump enable
- RD1,2 = X : reference divider ratio is selected through RDS input
- PSC = 1 : prescaler on
- OS = 0 : varicap enable

In 3-wire-bus mode the division ratio of the reference divider may be selected by applying an appropriate voltage at the RDS input pin 3.

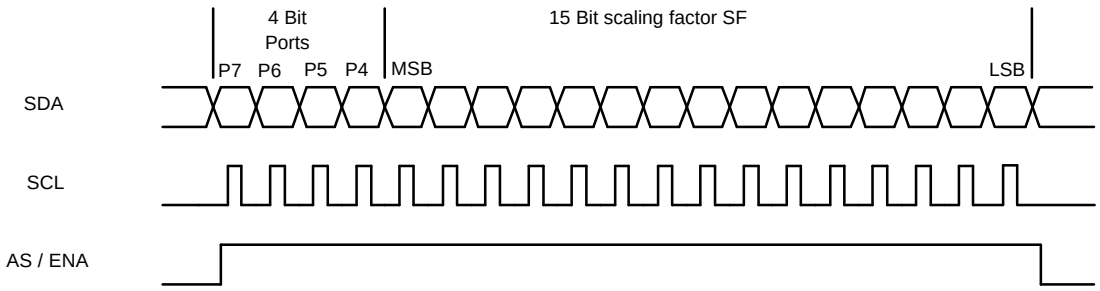
RDS : Reference divider selection pin 3

Reference divider ratio	Voltage at pin 3
1024	0 to 10% Vs
512	open or 40 to 60% Vs
640	90 to 100% Vs

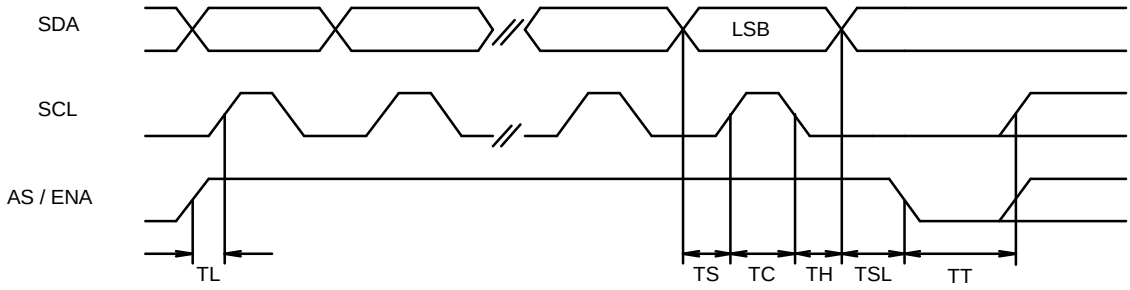
The complete PLL function can be disabled by programming a normally not used division ratio of zero. This allows the tuner alignment by supplying the tuning voltage directly through the 30V supply voltage of the tuner.

3 - WIRE - BUS DESCRIPTION (continued)

3 - WIRE - BUS PULSE DIAGRAM



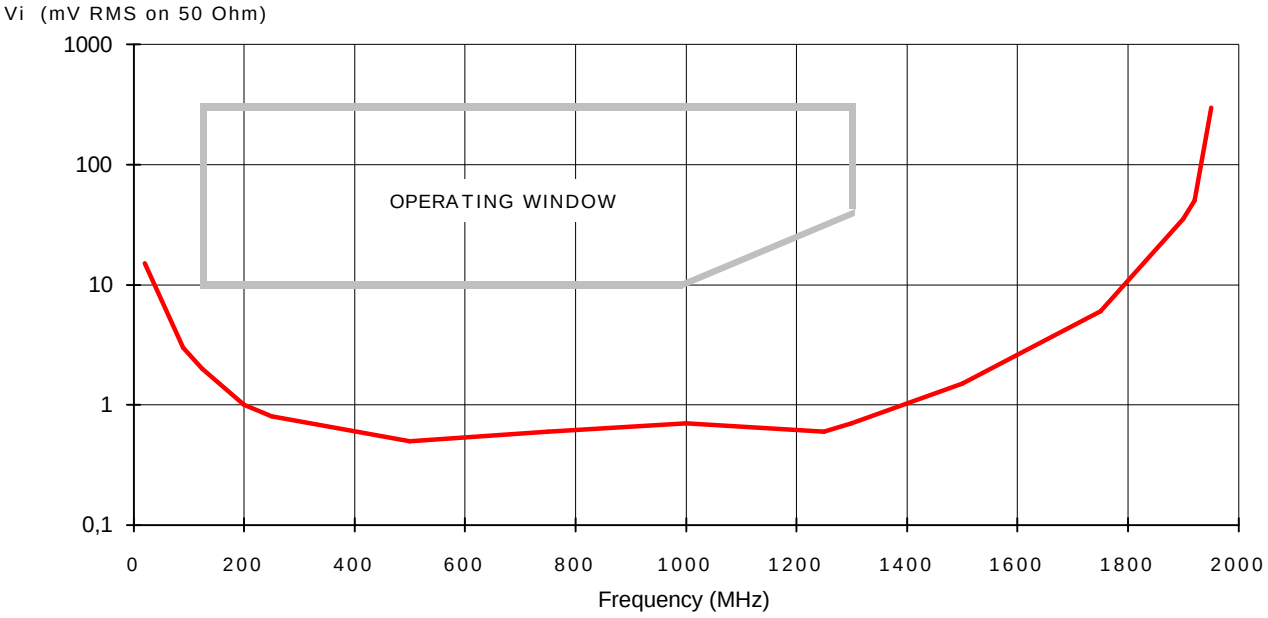
3 - WIRE - BUS TIMING



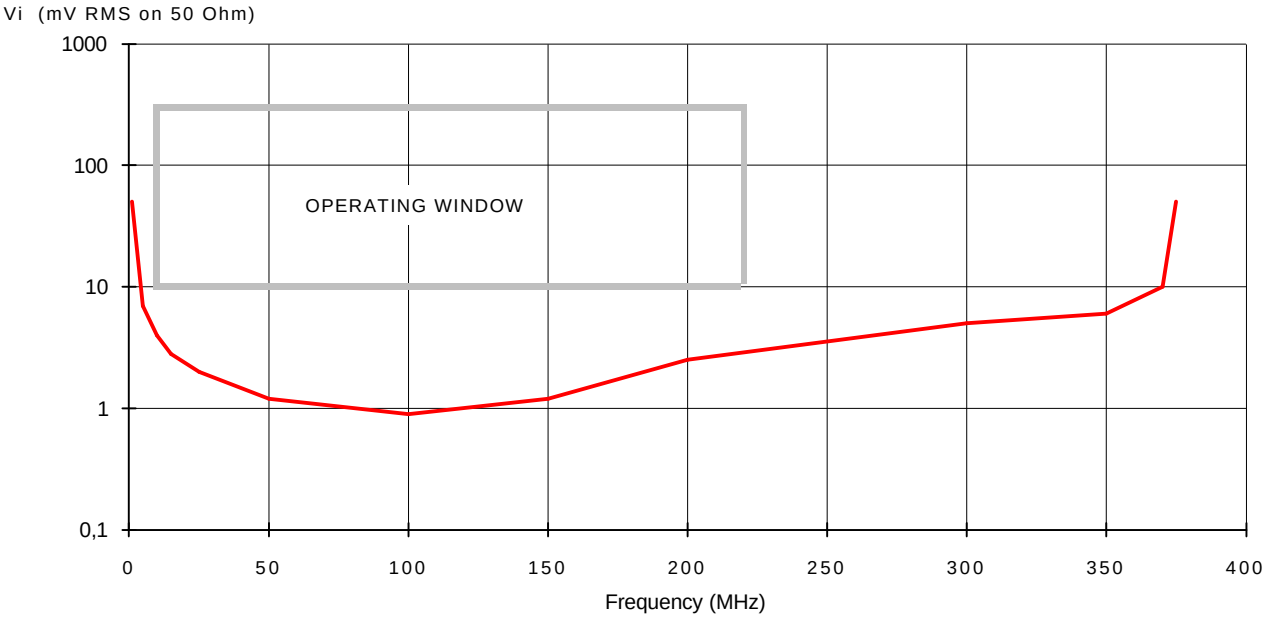
PARAMETER	SYMBOL	CONDITIONS	MIN.	MAX.	UNIT
Setup time	TS		2		us
Enable hold time	TSL		2		us
Clock width	TC		2		us
Enable setup time	TL		10		us
Enable between two transmissions	TT		10		us

Data hold time	TH		2		us

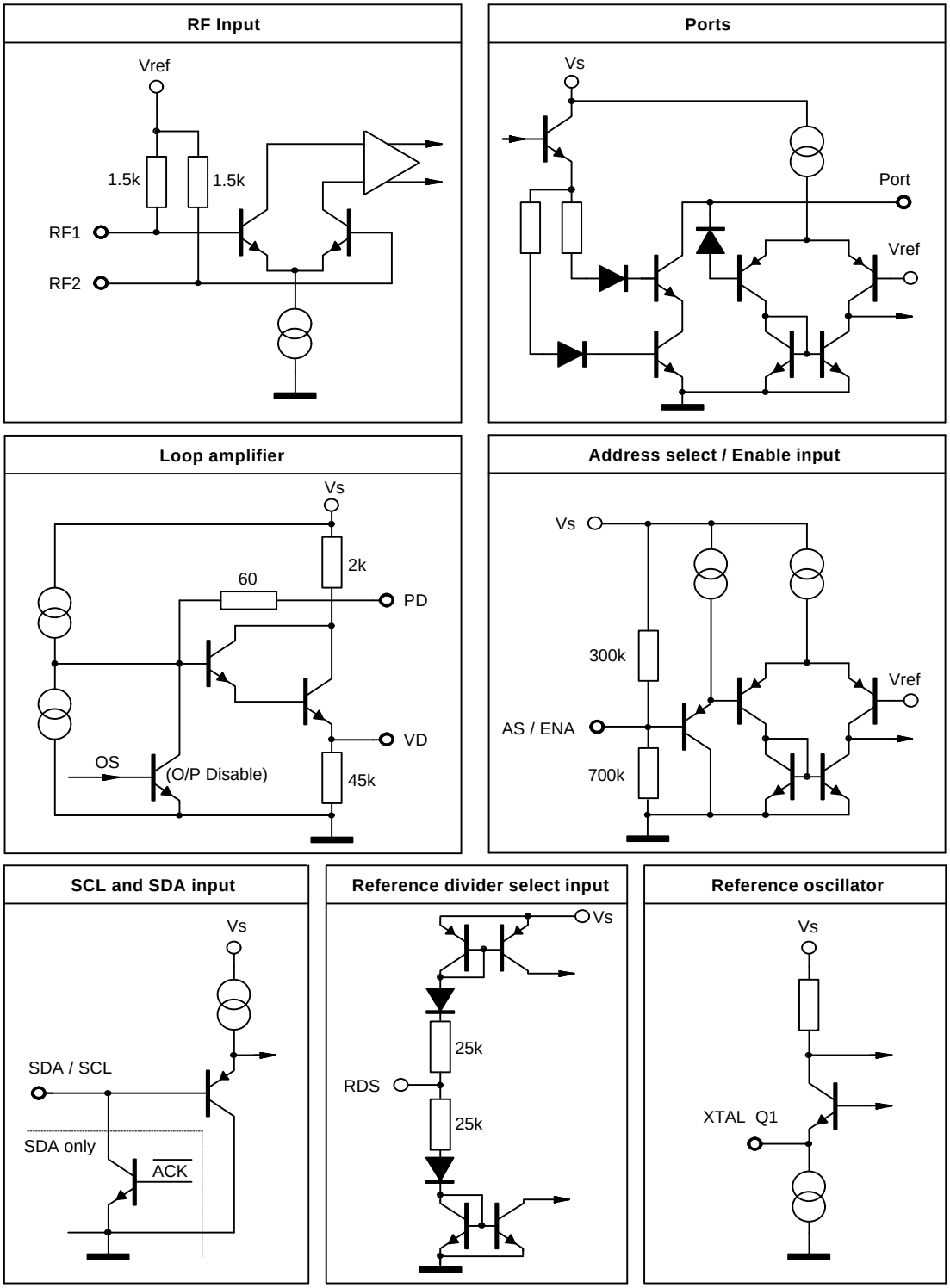
TYPICAL PRESCALER INPUT SENSITIVITY (Prescaler on : PSC = 1)



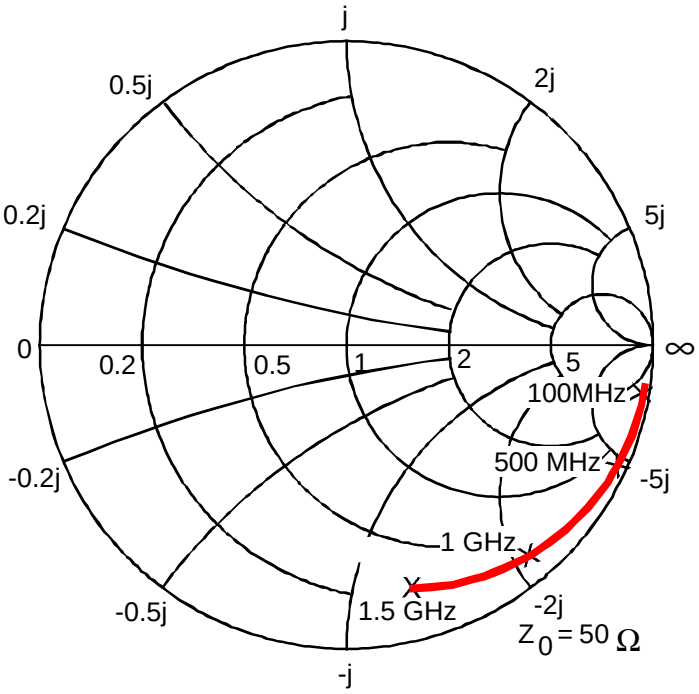
TYPICAL PRESCALER INPUT SENSITIVITY (Prescaler off : PSC = 0)



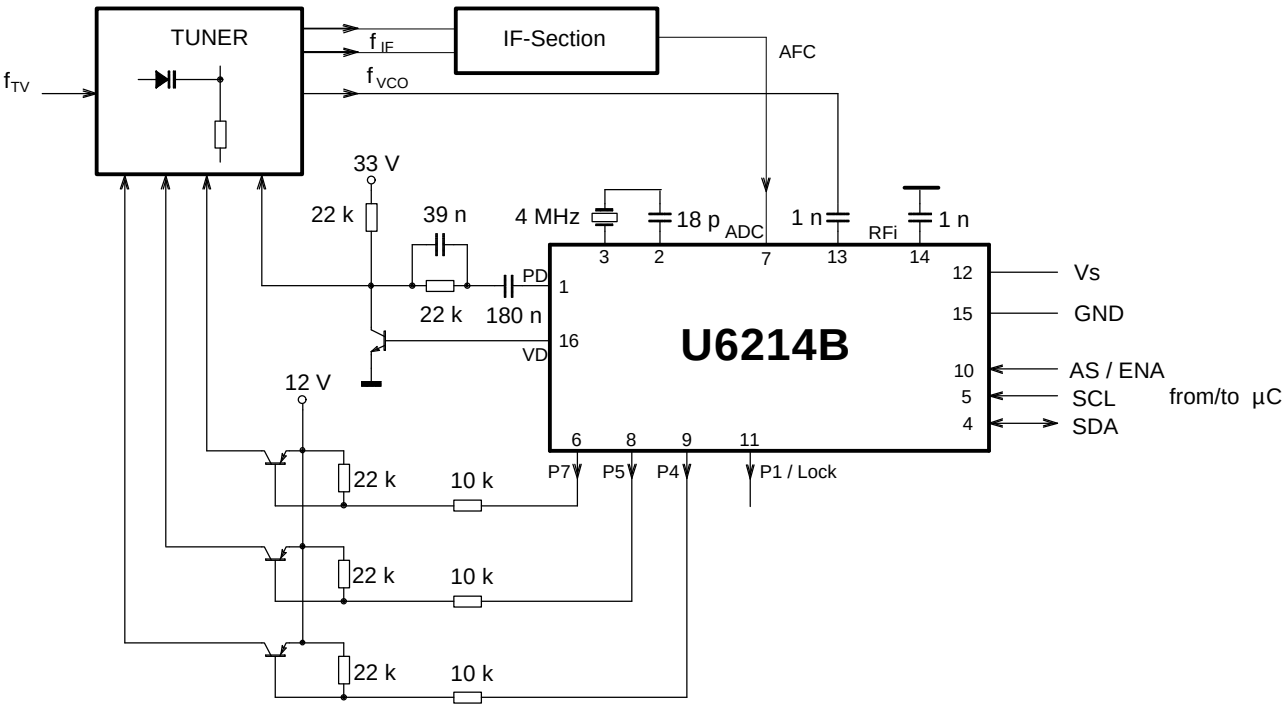
INPUT/OUTPUT INTERFACE CIRCUITS



TYPICAL INPUT IMPEDANCE



APPLICATION CIRCUIT



We reserve the right to make changes without further notice to improve technical design.